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Experimental and Analytical Characterization of Dual-Gated Germanium Junctionless p-Channel Metal–Oxide–Semiconductor Field-Effect Transistors

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The operation of germanium (Ge) dual-gated junctionless p-channel field-effect transistors (DG JL pFETs) is demonstrated. The top-gated hole mobility is approximately 120 $cm^2 \cdot V^{-1} \cdot s^{-1}$, which is close to the bulk mobility of p-type Ge with a doping concentration of 10^{19} cm^{-3}. The mobility has a weak hole density dependence and increases by applying a negative bottom gate voltage. In addition, simple analytical expressions for both the current–voltage characteristics and the threshold voltage in the linear region of the DG JL pFET are described. The result shows that normally-off Ge DG JL pFETs are achievable. Furthermore, the threshold voltage variation due to the random dopant number fluctuations in the channel is also discussed, which indicates that it can be reduced by decreasing the Ge and oxide thicknesses.

1. Introduction

The gate length scaling in metal–oxide–semiconductor field-effect transistors (MOSFETs) is becoming increasingly difficult because of the apparent increase in short-channel effects owing to a considerable reduction of the gate voltage controllability to the channel. To overcome these challenges, various device architectures, such as fully depleted silicon-on-insulator (FDSOI), double-gate MOSFETs, and multigate SOI MOSFETs have been proposed.[1–3] Nevertheless, not only the channel structure but also the ultrasharp and shallow source/drain (S/D) junction of nanometer-scale is of great concern, and imposes serious constraints on the doping techniques and thermal budget. A device that does not have any junctions, named the junctionless field-effect transistor (JL FET), was interestingly proposed by Colinge's group.[4,5] The doping concentration in the JL FET is uniform throughout the source (S), channel, and drain (D). Compared with the traditional inversion-mode MOSFETs, the JL FET has the following advantages. 1) It drastically simplifies the fabrication process. 2) It eliminates the lateral impurity diffusion and solves the problem of sharp doping profile formation. 3) It was demonstrated that the short-channel effects, such as drain-induced barrier lowering and subthreshold slope degradation, were improved when the device sizes were aggressively scaled down. 4) The mobility degradation in the high carrier density region is relaxed. 5) The gate dielectric thickness scaling is also relaxed in terms of the intrinsic delay time.

The electrical properties of such JL FETs have been reported in several publications.[6–13] However, all of them discussed silicon (Si) JL FETs. We have noted that germanium (Ge) intrinsically has much higher electron and hole mobilities than Si, even in the heavily doped region,[14] and that any metals are in good ohmic contact with p-type Ge because of the strong Fermi-level pinning near the Ge valence band edge.[15] Recently, we successfully fabricated a single-gated Ge JL pFET using germanium-on-insulator (GeOI), and demonstrated its FET operation by bottom gate sweeping.[16] On the other hand, both inversion- and accumulation-type Ge MOSFETs on GeOI have already been investigated, where the low impurity concentrations in Ge were used to achieve the higher carrier mobility. Furthermore, the metal S/D technology has been employed in pMOSFETs without any special technique,[17–21] because of the strong Fermi-level pinning, as mentioned above. In those viewpoints, the Ge JL pFET reported in this paper resembles the metal S/D GeOI pFETs with low impurity concentration so far reported. It should be, however, noted that the operational principle of the Ge JL FETs is quite different from that of the conventional metal S/D GeOI pFETs. Since the doping concentration of Ge in the metal S/D GeOI pFETs so far reported is very low, a sufficiently large gate voltage must be applied to form an accumulation or inversion layer with a high carrier concentration for achieving the on-state. All the generated carriers are confined to a very thin layer along the Ge/oxide interface owing to the strong electric field induced by the gate voltage. On the other hand, the doping concentration of Ge is extremely high in Ge JL FETs, and the carriers are uniformly located in the Ge film in the on-state. In fact, the on-state is in the flat band condition in terms of the energy band diagram of the gate stack. Thus, the electric field perpendicular to the current flow in the on-state of FETs is quite low for Ge JL pFETs, while it is quite high for the low-doped metal S/D GeOI pFETs. It is easily expected that in conventional metal S/D GeOI pFETs, the high perpendicular electric field should reduce the effective channel mobility owing to enhanced surface roughness scattering, whereas it is not the case in Ge JL FETs. Furthermore, the FET performance degradation in the on-state will be more significant in conventional metal S/D GeOI pFETs than in Ge JL FETs, because hot carriers generated by the high electric field in the channel will attack the interface and newly generate the interface states. In the JL FETs, however, the perpendicular electric field in the off-state should be high, and there are, in principle, no free carriers in the channel in the off-state. Thus, the interface will be less damaged in terms of hot carrier degradation. These facts will potentially be favorable for JL FETs. Thus it is important to investigate the characteristics of Ge JL FETs experimentally and analytically, though the reliability issue will not be included experimentally.

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In this paper, we first show Ge dual-gated (DG) JL pFETs fabricated on heavily doped GeOI. In addition, analytical expressions for the current–voltage (I–V) characteristics and the threshold voltage (V_{th}) in the linear region of the DG JL pFETs are described under the depletion layer approximation, because the random dopant number fluctuations (RDF) in conventional MOSFETs result in threshold voltage variation (ΔV_{th}), which increases with scaling down of the device.[22] Experimental studies also showed that in short-channel MOSFETs, the RDF-induced ΔV_{th} increased as the doping concentration increased.[23,24] However, in JL FETs, the channel doping concentration cannot be reduced in order to keep their inherent advantages. Thus, we finally discuss ΔV_{th} induced by RDF in the Ge DG JL FET based on the analytical model described in this paper.

2. Device Fabrication

A heavily gallium-doped GeOI wafer with 100-nm-thick buried SiO_2 was used. The substrate doping concentration was approximately $10^{19}\,cm^{-3}$, which was measured by the secondary ion mass spectroscopy (SIMS). Firstly, the initial 100-nm-thick Ge was thinned, by a wet-etching (H_2O_2) process, to approximately 60 nm, and mesa-type Ge islands with several lengths (60, 160, 260, 360, 460 μm) were defined. Next, Ge islands were thinned to approximately 15 nm only for the channel region, and 60-nm-thick Ge remained for the S/D regions to achieve good electrical contacts. After cleaning with methanol followed by HCl, 40 nm Y_2O_3 was deposited onto the Ge surface by sputtering, and then S/D contact holes were formed with a HCl-based solution. Next, a high-pressure oxidation (HPO) process was carried out at 550 °C for 10 min under O_2 pressure of 50 atm, and a 1–2-nm-thick layer of GeO_2 was formed after that. The superiority of the HPO process was reported previously.[25,26] Finally, Al was deposited and patterned as the top and bottom electrodes. Figures 1(a) and 1(b) show a schematic of the device and a typical cross-sectional transmission electron microscope (TEM) image of the Ge channel, respectively. The Ge thickness in the channel region was only 11 nm and good crystalline quality was maintained after the thinning process.

3. Results and Discussion

3.1 *I–V* characteristics and hole mobility in Ge DG JL pFETs

The source–drain current (I_{ds}) versus the top source–gate voltage ($V_{gs(top)}$) in the JL FET as a parameter of the bottom gate voltage (V_{BG}) is shown in Fig. 2, The source–drain voltage (V_{ds}) was −10 mV and the channel length (L) and width (W) were 160 and 130 μm, respectively. The on/off current (I_{on}/I_{off}) ratio was approximately 10^3, and the top-gated V_{th} was shifted to the positive direction by applying a negative V_{BG}. This is because a negative V_{BG} can increase the total mobile carrier number in the channel. When a larger negative V_{BG} is applied, a larger positive $V_{gs(top)}$ is needed to fully deplete the channel.

The carrier mobility is an important parameter for characterizing the device performance. To estimate the effective carrier mobility, we performed the split capacitance–voltage (C–V) measurement between the gate and S/D. Figure 3 shows the frequency dependence of the split

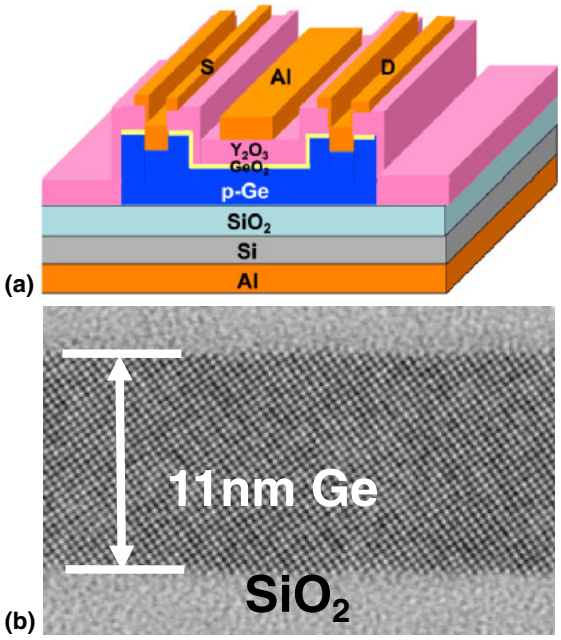

Fig. 1. (Color online) (a) Schematic of the dual-gated junctionless Ge MOSFET structure. (b) Cross-sectional TEM image of ultrathin GeOI. Ge thickness is only 11 nm and a good crystalline quality is maintained after the thinning process.

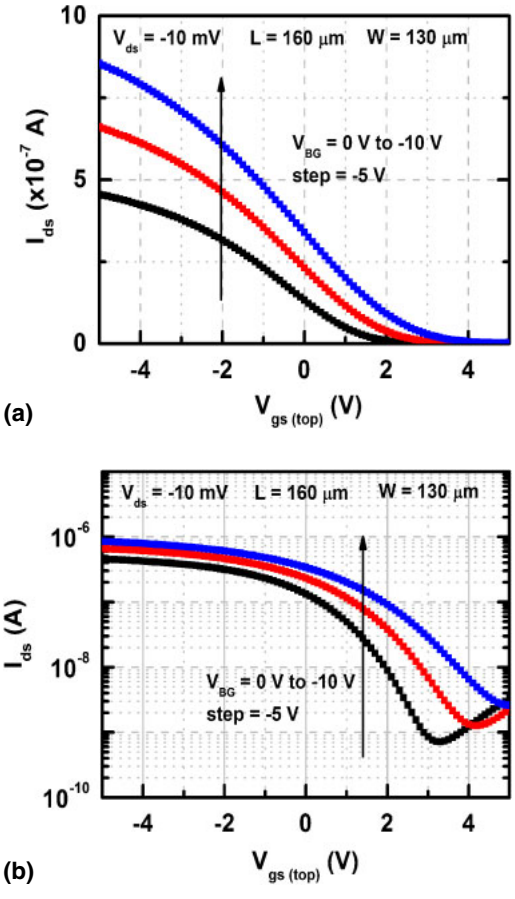

Fig. 2. (Color online) Both (a) linear and (b) subthreshold characteristics of I_{ds}–$V_{gs(top)}$ in JL FET at $V_{ds} = -10$ mV as a function of bottom gate voltage V_{BG}. V_{th} is shifted by changing V_{BG}, whereas the I_{on}/I_{off} ratio is 10^3 owing to a relatively weak confinement in planar dual gates.

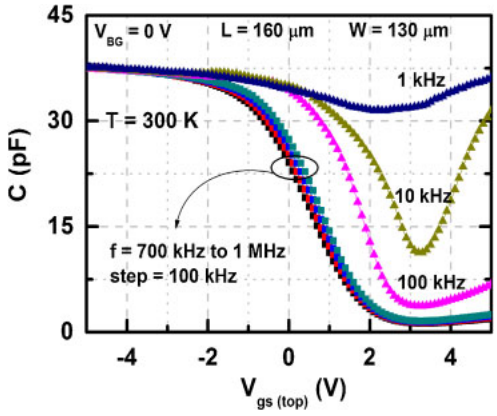

Fig. 3. (Color online) Frequency dependence of the split C–V characteristics when the top gate voltage is swept and the bottom gate is grounded. High-frequency (1 MHz) C–V curve shows a clear depletion, whereas the low-frequency one (1 kHz) shows almost no capacitance change with top gate voltage.

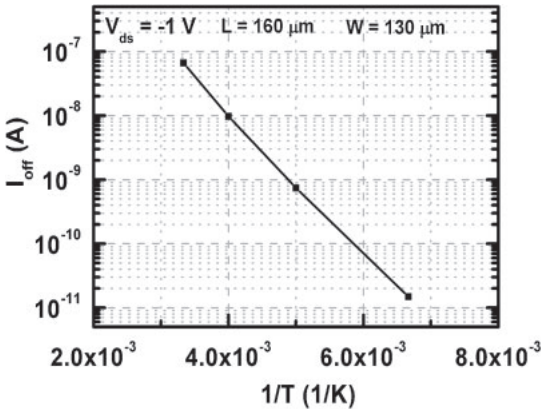

Fig. 5. Arrhenius plot of the off-state leakage current as a function of the reciprocal of measurement temperature. Since the activation energy is estimated to be 0.2 eV, the off-state leakage current is expected to be due to the carriers generated through the Hall–Shockley–Read generation-recombination centers that lie 0.2 eV from the nearest allowed band.

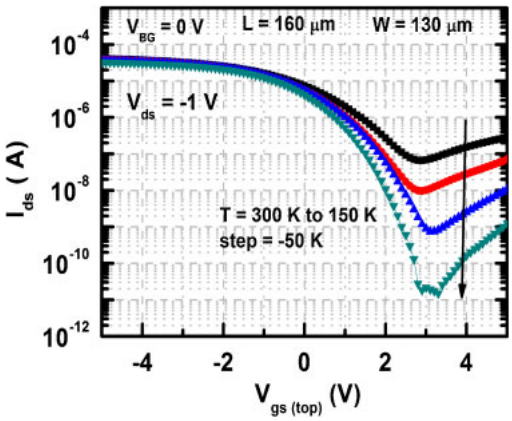

Fig. 4. (Color online) I_{ds}–$V_{gs(top)}$ characteristics with the bottom gate grounded at 300, 250, 200, and 150 K. It is clear that the leakage current is significantly reduced when the temperature is decreased.

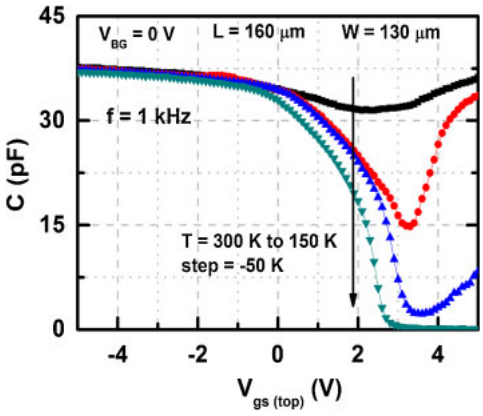

Fig. 6. (Color online) Split C–V characteristics in the low-frequency (1 kHz) measurement at 300, 250, 200, and 150 K. The capacitance in the depletion region decreases as the temperature decreases. This result supports our view that the minority carrier generation in the channel at room temperature may hinder the depletion capacitance.

C–V characteristics when $V_{gs(top)}$ was swept and the bottom gate was grounded. It is interesting that the high-frequency (1 MHz) C–V curve shows a clear depletion, whereas the low-frequency one (1 kHz) shows almost no capacitance change upon sweeping $V_{gs(top)}$. It was inferred that generation-recombination might occur at the depletion edge, and in the channel, the generated minority carriers (electrons) were accumulated at the MOS interface in the low-frequency C–V. To confirm our view on this result, we measured I_{ds}–$V_{gs(top)}$ and C–$V_{gs(top)}$ characteristics at four temperatures (300, 250, 200, and 150 K). As shown in Fig. 4, the off-state leakage current is significantly reduced when the temperature is decreased. Figure 5 presents the Arrhenius plot of the off-state leakage current as a function of the reciprocal of temperature, which indicates that the off-state leakage current is in proportion to $\exp(-E_A/k_BT)$, where k_B is the Boltzmann constant, T is the temperature, and E_A is the activation energy. From the slope in Fig. 5, E_A is estimated to be approximately 0.2 eV. This shows that the current carried by the carriers generated through the Hall–Shockley–Read generation-recombination centers that lie 0.2 eV above the valence band or below the conduction band in the space-charge region is predominant in the off-state current. Hall[27] and Pell[28] also showed similar experimental data for the position of the Hall–Shockley–Read generation-recombination centers with the values of 0.22 and 0.3 eV from the nearest allowed band in Ge. Thus, the off-state leakage current can be reduced by careful optimization of the sample fabrication procedure and heavily doped GeOI wafer formation process. The split C–V characteristics in the low-frequency (1 kHz) measurement at 300, 250, 200, and 150 K are shown in Fig. 6. The capacitance in the depletion region decreases as the temperature decreases. This result also supports our view that the generation of electrons in the channel at room temperature may hinder the depletion capacitance, as mentioned above.

Therefore, in order to estimate the mobile carrier number in JL FETs using the split C–V, we employed the high-frequency C–V results. In fact, the capacitance was independent of the frequency above 700 kHz. The split C–V characteristics for various V_{BG} at 1 MHz are shown in Fig. 7. The parallel shift of capacitance with V_{BG} may be

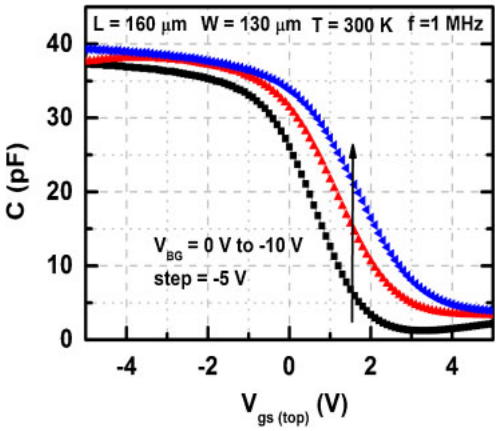

Fig. 7. (Color online) Split C–V characteristics for three kinds of bottom gate voltages under a high frequency of 1 MHz.

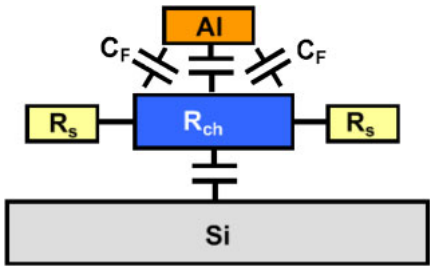

Fig. 8. (Color online) Schematic equivalent circuit of FET in the present experiment. The parasitic fringing capacitance (C_F), series resistance (R_S), and channel resistance (R_{ch}) are shown.

due to the modulation of the mobile carrier number by V_{BG}, which is similar to the reason for the V_{th} shift.

Figure 8 shows the equivalent circuit of our Ge DG JL FET, where the parasitic fringing capacitance (C_F), series resistance (R_S), and channel resistance (R_{ch}) are denoted. The contribution of the fringing parasitic capacitance to the total gate capacitance was very small because the channel length and width were very large (160 and 130 μm, respectively). On the other hand, the parasitic series resistance, which included S/D offset and contact resistances, was very large and should be considered to accurately estimate the mobility. Therefore, we estimated the series resistances from the relationship between the measured total resistance and the gate length using thin Ge resistors with different gate lengths under the top gate floating condition. After the parasitic resistance correction, the top-gated effective hole mobility was calculated. The results for $V_{BG} = 0$, -5, and -10 V are shown in Fig. 9. The top-gated mobility is approximately $120\,cm^2 \cdot V^{-1} \cdot s^{-1}$ for $V_{BG} = 0$, which is close to the bulk mobility of p-type Ge with a doping concentration of $10^{19}\,cm^{-3}$. In addition, the top-gated mobility in Fig. 9 shows a relatively weak hole density (N_s) dependence. These findings are in accordance with our previous results for the single bottom-gated JL FETs.[16] They are beneficial points of JL FETs. Furthermore, we found that the mobility increased as the bottom gate was applied in the negative direction, and the top-gated hole mobility was approximately $160\,cm^2 \cdot V^{-1} \cdot s^{-1}$ for $V_{BG} = -10$ V. The enhancement of mobility by DG mode operation

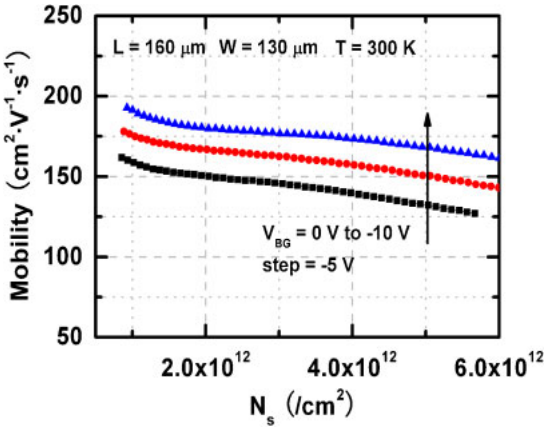

Fig. 9. (Color online) Top-gated mobility as a function of hole density at $V_{BG} = 0$, 5, and -10 V. The top-gated mobility is approximately $120\,cm^2 \cdot V^{-1} \cdot s^{-1}$ at $V_{BG} = 0$, which is close to the bulk mobility of p-type Ge with the doping concentration of $10^{19}\,cm^{-3}$. The mobility shows relatively weak dependence on the hole density, but increases when V_{BG} is changed from 0 to -10 V.

in the conventional undoped or lightly doped Si has been investigated and discussed from the viewpoints of the average effective mass reduction in the DG mode because of the increased population in the light hole band[29] or carrier scattering reduction from the SiO_2 roughness and/or the charged interfaces states in the two-dimensional carrier gas in DG mode operation.[30] In the present DG JL FET case, however, the valence band structure cannot be simply modeled because of band-gap narrowing in heavily doped semiconductors. Therefore, it is not appropriate to apply the conventional mobility discussion to the JL FETs. Instead, we qualitatively discuss the electric field effect of the negative bottom gate on top surface band bending. Figures 10(a) and 10(b) show the schematic band diagrams for the Ge DG JL pFET when the channel is in the on-state owing to a negative $V_{gs(top)}$ with $V_{BG} = 0$ and $V_{BG} < 0$, respectively. When a negative bottom gate voltage is applied, as shown in Fig. 10(b), the top electric field is reduced while the bottom electric field is slightly increased. Therefore, the top-gated mobility is likely to effectively increase. The effective mass and/or the scattering modulations upon bottom gate voltage application should obviously be considered. Also, the effect of V_{BG} on the parasitic resistance should be more carefully taken into account experimentally before quantitative discussion, though we have taken account of it in the first-order approximation. To understand the physical origin more clearly, further research is needed.

3.2 Analytical model of *I*–*V* characteritics in Ge DG JL pFETs

In JL FETs, the channel doping concentration cannot be reduced in order to keep their inherent advantages, and the conductance in the heavily doped channel may be different from that in conventional MOSFETs with lightly doped channels. Generally speaking, JL FETs are likely to behave as normally-on devices. In addition, it is well understood that RDF induces a large ΔV_{th} in conventional MOSFETs with heavily doped channels. Thus, we first derive an analytical model of V_{th} in the Ge DG JL FET in the linear

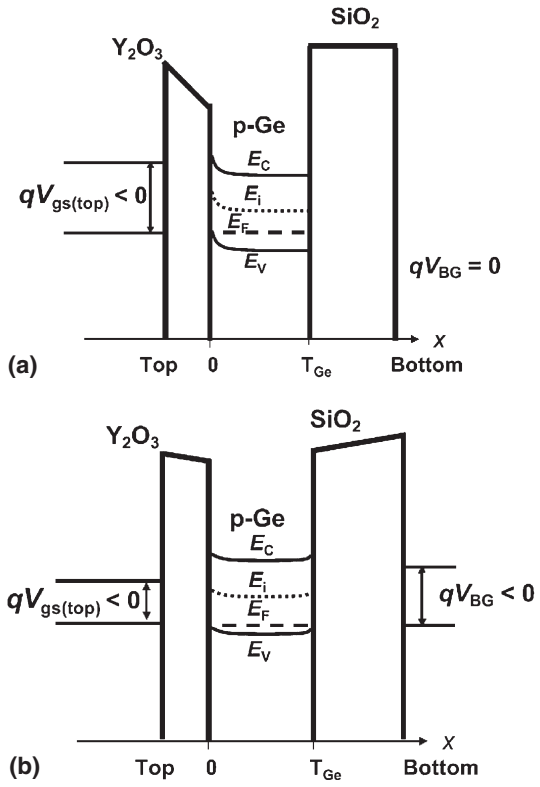

Fig. 10. Schematic energy band diagrams for Ge DG JL pFET when the channel is accumulated by negative $V_{gs(top)}$ with (a) $V_{BG} = 0$, and (b) $V_{BG} < 0$. It is expected that the internal electric field is relaxed by applying negative bottom gate voltage.

region under the depletion layer approximation. Then ΔV_{th} is discussed by assuming a Gaussian distribution of the dopant number in the channel.

Here, we focus on a symmetric DG FET structure that consists of a heavily doped ultrathin p-type Ge layer with symmetric top and bottom gate stacks. In this model, we consider the effects of depletion layers on the channel from the bottom and the top independently.

3.2.1 Possibility of normally-off Ge DG JL FETs

In the conventional MOSFETs, V_{th} is defined under the condition of $2\Psi_B$ band bending of the surface potential associated with depletion layer formation. Here, $q\Psi_B$ is the energy difference between the intrinsic Fermi level and the Fermi level, and q is the electron charge. In the JL FETs, V_{th} is defined as the gate voltage when the Ge channel is fully depleted. In the symmetric DG JL FET case, the channel becomes the off-state when the depletion layer width formed by each gate reaches half the Ge thickness. The depletion layer width in the Ge layer can be easily found and expressed as

$$T_{dep} = -\frac{\varepsilon_{Ge}}{C_{ox}} + \frac{\varepsilon_{Ge}}{C_{ox}}\sqrt{1 + 2\frac{{C_{ox}}^2}{\varepsilon_{Ge}}\frac{V_{gs} - V_{FB}}{qN_A}}, \quad (1)$$

where ε_{Ge} is the Ge permittivity, N_A is the channel doping concentration, V_{gs} is the source–gate voltage, V_{FB} is the flatband voltage, and $C_{ox} = \varepsilon_{ox}/T_{ox}$, where ε_{ox} is the oxide permittivity and T_{ox} is the gate oxide thickness. The current through the channel should satisfy Ohm's law in the linear region, thus the current can be expressed as

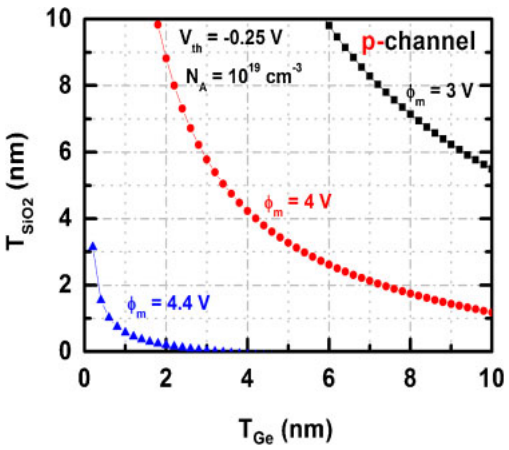

Fig. 11. (Color online) Relationship between T_{SiO_2} and T_{Ge} under $N_A = 10^{19}\,cm^{-3}$ for achieving $V_{th} = -0.25\,V$. A normally-off p-channel FET ($V_{th} = -0.25\,V$) is obtainable by employing proper thicknesses of Ge and SiO_2 together with small-work-function metals such as Al and W that have work functions close to 4.1 and 4.4 eV, respectively. $q\phi_m$ is the work function of the metal.

$$I_{ds} = \frac{\mu q N_A (T_{Ge} - 2T_{dep}) V_{ds} W}{L}, \quad (2)$$

where T_{Ge} is the Ge thickness and μ is the carrier mobility in the channel, and V_{ds} is the source–drain voltage.

In the accumulation region, the source–drain current I_{ds} consists of two parts. One is the body current and the other is the accumulation current. In this paper, however, since we focus on the near V_{th} region, we will not discuss the over-threshold region.

It is reasonable to define V_{th} as the gate voltage when $I_{ds} = 0$, Thus, by combining eqs. (1) and (2), V_{th} can be expressed as

$$V_{th} = V_{FB} + \frac{qN_A{T_{Ge}}^2}{8\varepsilon_{Ge}} + \frac{qN_A T_{Ge}}{2C_{ox}}. \quad (3)$$

Since the device reported in the present experiment was the normally-on FET, as shown in Fig. 7, the question is whether it is possible to achieve the normally-off Ge JL FETs by optimizing device parameters in the DG structure. Figure 11 shows the relationship between T_{SiO_2} and T_{Ge} when $N_A = 10^{19}\,cm^{-3}$ and $V_{th} = -0.25\,V$ was assumed. By employing appropriate Ge and SiO_2 thicknesses together with a low-work-function metal, for example, Al and W with work functions close to 4.0 and 4.4 eV, respectively,[31] we can achieve the normally-off Ge DG JLFET. Here, we simply assume that there are no interface traps or oxide charges, and that qV_{FB} is equal to the work function difference between the gate electrode and Ge.

3.2.2 ΔV_{th} due to RDF in Ge DG JL pFETs

Since ΔV_{th} induced by RDF is a major concern in the conventional MOSFETs with heavily doped channels, now we discuss it in Ge DG JL FETs, where the channel doping concentration is much higher than the usual doping concentration in conventional MOSFETs. We assume the dopant number fluctuations can be described by the Gaussian distribution and discuss ΔV_{th} in terms of the standard deviation of the dopant number in the channel.

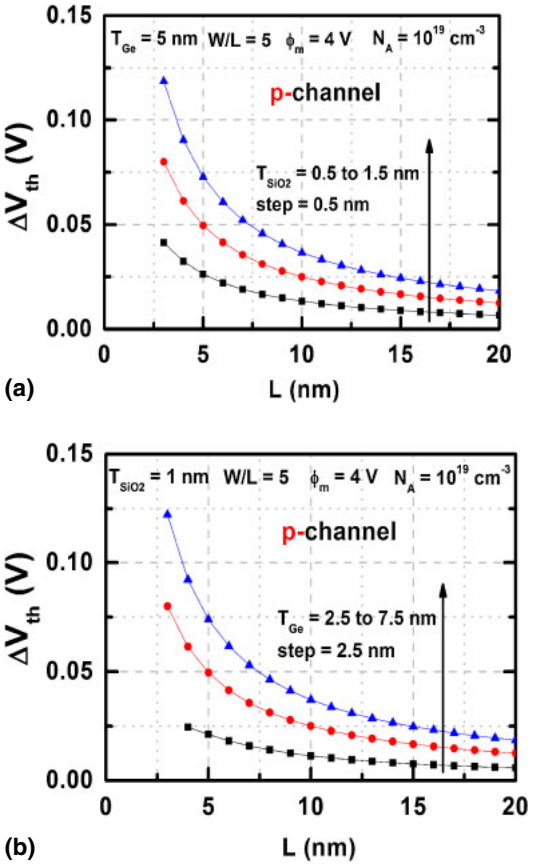

Fig. 12. (Color online) The threshold voltage variation ΔV_{th} in Ge DG JL p-FET as a function of channel length L with different (a) oxide (SiO_2) thickness and (b) Ge thickness. ΔV_{th} is roughly 25 mV when $L = 10$ nm if Ge and oxide thicknesses of 5 and 1 nm, respectively, are assumed. By reducing T_{Ge} and T_{SiO_2}, ΔV_{th} is significantly reduced.

Therefore, the dopant number n in the channel is expressed as

$$n = N_A T_{Ge} L W. \tag{4}$$

The standard deviation of the dopant number fluctuations, σ, in the channel is considered to be

$$\sigma = \sqrt{n} = \sqrt{N_A T_{Ge} L W}, \tag{5}$$

when the fluctuations follow the Gaussian distribution. Then, the actual dopant number in the channel should be in the range of $n' = n \pm \sqrt{n}$. Thus, the real doping "concentration" can be described as

$$N_{A1} \approx \frac{N_A T_{Ge} L W + \sqrt{N_A T_{Ge} L W}}{T_{Ge} L W}, \qquad N_{A2} \approx \frac{N_A T_{Ge} L W - \sqrt{N_A T_{Ge} L W}}{T_{Ge} L W}. \tag{6}$$

By substituting the above equation into the V_{th} definition eq. (3), we can get two threshold voltages. ΔV_{th} is defined as half the absolute value of the difference between them. Figures 12(a) and 12(b) show ΔV_{th} versus L as a parameter of T_{SiO_2} and T_{Ge} in a Ge DG JL pFET. ΔV_{th} is roughly 25 mV when $L = 10$ nm, if T_{Ge} and T_{SiO_2} are 5 and 1 nm, respectively. This fact suggests that ΔV_{th} due to RDF should be of concern in JL FETs. However, a good thing is that ΔV_{th} can be controlled by adjusting T_{Ge} and T_{SiO_2}. By reducing T_{Ge} and T_{SiO_2}, ΔV_{th} is significantly reduced.

4. Conclusions

The operation of the Ge DG JL pFETs fabricated on heavily doped GeOI substrates was demonstrated. The I_{on}/I_{off} ratio was approximately 10^3 at present, and the top-gated V_{th} was shifted by changing the bottom gate voltage V_{BG}. The off-state leakage current was described by an Arrhenius-type conduction with the activation energy of approximately 0.2 eV. This finding strongly suggests that the off-state leakage current is due to the carriers generated through the Hall–Shockley–Read generation-recombination centers that lie 0.2 eV above the valence band or below the conduction band in the space-charge region. The split C–V method was used for hole mobility extraction, and the top-gated mobility was approximately $120\,cm^2 \cdot V^{-1} \cdot s^{-1}$ for $V_{BG} = 0$, which is close to the bulk mobility of p-type Ge with the doping concentration of $10^{19}\,cm^{-3}$. In addition, we found that the mobility showed weak hole density dependence compared with that in the inversion-type FETs, and that the negative bottom gate voltage application in DG JL FET enhanced the mobility. These results will be partly understandable considering the fact that the carrier conduction in the bulk, rather than that at the interfaces, is dominant in JL FETs, though further study is needed to enable quantitative discussion.

Furthermore, the analytical expressions for I–V characteristics and V_{th} in the Ge DG JL pFET were derived. The results show that the normally-off Ge DG JL pFET is achievable. We also estimated RDF-induced ΔV_{th} in Ge DG JL pFET to be roughly 25 mV when the channel length is 10 nm by choosing T_{Ge} and T_{SiO_2} of 5 and 1 nm, respectively. In addition, ΔV_{th} can be further reduced by optimizing T_{Ge} and T_{SiO_2} or by changing the device structure to a trigate or gate-all-around FET. Thus, the advantages of Ge JL FETs make it a promising candidate for future electron device applications.

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